

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

- 1 1. A method of adjusting carrier mobility in
2 semiconductor devices comprising the steps of
3 depositing a metal or combination of metals to
4 contact one of a first or second transistor gate
5 structure, and
6 alloying said metal and said transistor gate
7 structure to form a first stressed alloy within said
8 transistor gate whereby a first stress is created in
9 at least one corresponding channel of said first or
10 second transistors without producing a stress in at
11 least one channel of the other transistor of said
12 first or second transistors.
- 1 2. A method as recited in claim 1 in which said
2 alloy is a silicide.
- 1 3. A method as recited in claim 1 in which first
2 transistor and second transistor are of opposite
3 conductivity types.
- 1 4. A method as recited in claim 3 comprising
2 further the steps of
3 depositing a metal over said first transistor
4 gate and not over said second transistor gate to
5 alloy with a first electrode to form said first
6 stressed alloy causing a first stress to be applied
7 in at least one channel of said first transistor,
8 and

9 depositing a metal over said second transistor
10 gate and not over said first transistor gate to
11 alloy with a second electrode to form a second
12 stressed alloy causing a second stress to be applied
13 in at least the channel of said second transistor.

1 5. A method as recited in claim 4 in which said
2 first stressed alloy and second stressed alloy apply
3 opposing stresses.

1 6. A method as recited in claim 5 in which
2 said first stress caused by said first stressed
3 alloy exhibits stress in at least the channel region
4 of said first transistor opposite to the stress
5 provided by said first stressed alloy, and
6 said second stress caused by said second
7 stressed alloy exhibits stress in at least the
8 channel region of said second transistor opposite to
9 the stress provided by said second stressed alloy.

1 7. A method as recited in claim 6 wherein the
2 carrier mobility is regulated by applying tensile
3 stress to at least one channel of said first
4 transistor while applying compressive stress to at
5 least one channel of said second transistor.

1 8. A method as recited in claim 1 wherein said
2 depositing step comprises
3 depositing a first metal to a portion of said
4 gate electrode material in said first transistor to
5 form a third alloy at the lower region of the gate
6 electrode proximate to the channel of said first
7 transistor; and
8 depositing a second metal over said first

9 transistor gate electrode to form said first
10 stressed alloy within first transistor gate in the
11 upper region of the gate electrode.

1 9. A method as recited in claim 8 wherein said
2 depositing step further comprises
3 depositing a third metal to a portion of said
4 gate electrode material in said second transistor to
5 form a fourth alloy at the lower region of the gate
6 electrode proximate to the channel of said second
7 transistor; and
8 depositing a fourth metal over said second
9 transistor gate electrode to form said second
10 stressed alloy within second transistor gate in the
11 upper region of the gate electrode, whereby said
12 second stressed alloy creates a second stress to the
13 channel area of said second transistor.

1 10. A method as recited in claim 9 wherein the
2 first stressed alloy and second stressed alloy are
3 of opposing stresses.

1 11. A method as recited in claim 10 wherein the
2 first transistor and second transistor are of
3 opposite conductivity types.

1 12. A method as recited in claim 11 wherein
2 said first transistor is an nFET wherein said
3 first stressed alloy is compressive creating said
4 first stress wherein first stress is tensile, and
5 said second transistor is a pFET wherein said
6 second stressed alloy is tensile creating said
7 second stress wherein second stress is compressive.

1 13. An apparatus that adjusts carrier mobility in
2 semiconductor devices comprising:
3 a substrate,
4 a first transistor having a gate dielectric,
5 gate electrode, and source, drain, and gate regions,
6 formed on said substrate,
7 a second transistor having a gate dielectric,
8 gate electrode, and source, drain, and gate regions,
9 formed on said substrate, and
10 a first stressed alloy providing tensile stress
11 at least in one channel of first transistor.

1 14. An apparatus as recited in claim 13 in which
2 said alloy is a silicide.

1 15. An apparatus as recited in claim 13 further
2 comprising a second stressed alloy providing
3 compressive stress at least in one channel of second
4 transistor.

1 16. An apparatus as recited in claim 15 wherein
2 said first and second stressed alloys can be
3 composed of SiNi, CoSi₂, PdSi, or other material
4 that exhibits either tensile or compressive
5 properties.

1 17. An apparatus as recited in claim 16 further
2 comprising:
3 a third alloy located in the lower region of
4 the gate area of said first transistor, and
5 a fourth alloy located in the lower region of
6 the gate area of said second transistor.

1 18. An apparatus as recited in claim 17 in which

2 the gate electrode wraps around at least two sides
3 of said channel of each of said first and second
transistors.

1 19. An apparatus as recited in claim 13 wherein the
2 first stressed alloy can be composed of SiNi, CoSi₂,
3 PdSi, or other material that exhibits either tensile
4 or compressive properties.

1 20. An apparatus as recited in claim 19 in which the
2 gate electrode wraps around at least two sides of
3 said channel of each of said first and second
4 transistors.